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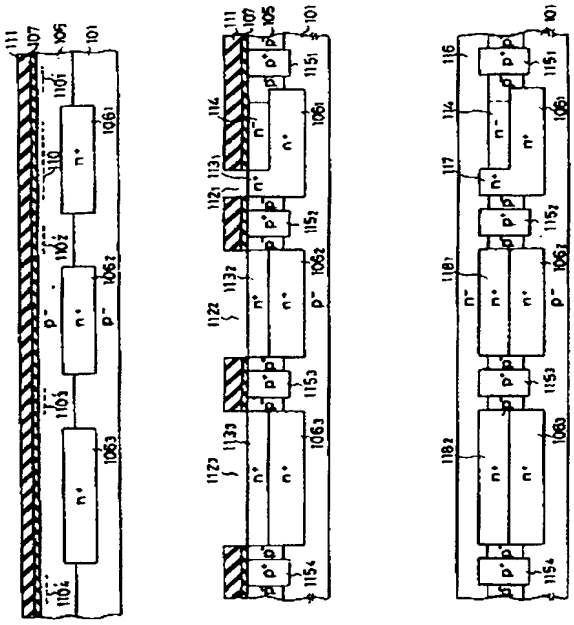
TITLE : SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To make high-dielectric strength elements and high-speed elements to coexist, by a method wherein p epitaxial and n epitaxial layers are overlaid on a $p^-$ type Si substrate, two layers are buried around the interfaces between the substrate and p epitaxial layer, and between both epitaxial layers, and $p^+$ layers are formed extending from the p epitaxial layer to the substrate as a part of detached layer of the n epitaxial layer.

CONSTITUTION: $N^+$ layers 106 are buried around the interfaces between a $P^-Si$ substrate 101 and a $p^-$ epitaxial layer 105. P ions and B ions are implanted in the layer $106_1$, and between layers, respectively, and they are convered by $SiO_2$111. windows 112 are selectively opened for thermal diffusing As so as to form $n^+$ layers 113, $n^-$ layers 114 in layers 110, and $p^+$ layers 115 extending from layers 110' to the substrate. Thin films 111 and 107 are, then, removed, and an $n^-$ epitaxial layer 116 is overlaid thereonto so that $n^+$ layers 117 and 118 are generated by the self-doping. After this, $p^+$ layers 119 are provided for coupling with layers 115. High dielectric strength and high speed $I^2L$ devices are, then, formed in the regions $116_1$ to $116_3$ by a conventional method. In this structure, a highly integrated device in which high performance, high dielectric strength and high speed elements are coexistable can be provided.

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